REMARKS

Claim 6 is rejected under 35 USC §112, second paragraph, because the Examiner asserts that the tradenames "SiLK, Teflon, parylene-N, parylene-F and Flare" need to describe a particular material or product. Claim 6 is amended herein.

Claims 1-2 and 17-18 are rejected under 35 USC §102(b), as allegedly being anticipated by Matumoto (US 5,893,749).

Claims 1-2, 4-6 and 17-20 are rejected under 35 USC §102(e), as allegedly being anticipated by Ho et al. (US 2002/0108929 A1, hereinafter "Ho").

Claim 3 is rejected under 35 USC §103(a), as allegedly being unpatentable over Ho in view of Demmin et al. (US 6,635,185, hereinfter "Demmin").

Claims 7-12 are rejected under 35 USC §103(a), as allegedly being unpatentable over Ho in view of Hsieh et al. (US 2003/0109143, hereinfter "Hsieh").

Applicants respectfully traverse the §§ 102(b), 102(e) and 103(a) rejections with the following arguments.

35 U.S.C. § 102(b)

Matumoto

Applicants respectfully contend that Matumoto does not anticipate independent claims 1 and 17 because Matumoto does not teach each and every feature of these claims.

For example, Matumoto does not teach forming an at least one conductive feature within the first and second layers; and performing a process to clean an exposed surface of the conductive feature, wherein the process forms a recess in the first layer in the region where the second layer is not covering the first layer, as recited in claim 1 of the present application.

The Examiner claims that Matumoto shows a first layer 13, a second layer 14, 15 and a recess 13A. The recess 13A is filled with a conductive material 16, however, Matumoto teaches nothing after the conductive material 16 is deposited. There is no mention of a process to clean an exposed surface of the conductive material, much less the formation of a recess in the first layer in the region where the second layer is not covering the first layer during the process, as required by claim 1 of the present invention.

Similalry, Matumoto fails to teach performing a preclean process on a surface of the first wiring level, wherein the preclean process forms a recess within the first layer in a region of the first wiring level where the second layer does not cover the first layer, and forming a second wiring level on a surface of the first wiring level comprising a third layer on the surface of the first wiring level and a plurality of conductive features within the third layer, wherein the recess within the first layer of the first wiring level is replicated producing an electrical short between at least two of the plurality of conductive features within the second wiring level, as required by

claim 17 of the present invention.

Again, there is no mention in Matumoto of a preclean process forming a recess within the first layer, rather the recess of Matumoto is formed using conventional photoresist processes (see, col. 4, lns. 10-12). In addition, Matumoto does not teach forming a third layer on the surface of layers 14, 15 having a plurality of conductive features, much less the replication of the via hole formed in layer that produces an electrical short between at least two conductive features within the third layer.

Therefore, Applicants respectfully maintain that Matumoto does not anticipate claims 1 and 17, and that claims 1 and 17 are in condition for allowance. Furthermore, since claims 2-12 depend from claim 1 and claims 19-21 depend from claim 17, Applicants contend that claims 2-12 and 19-21 are likewise in condition for allowance.

Ho

Applicants respectfully contend that Ho does not anticipate independent claims 1 and 17 because Ho does not teach each and every feature of these claims.

For example, Ho does not teach forming an at least one conductive feature within the first and second layers; and performing a process to clean an exposed surface of the conductive feature, wherein the process forms a recess in the first layer in the region where the second layer is not covering the first layer, as recited in claim 1 of the present application.

The Examiner claims that Ho shows a first layer 14, a second layer 12 and a recess formed using an etching process. Applicants assert that there is no conductive feature formed in

Ho prior to the formation of the recess. Likewise, there is no mention in Ho of a process to clean an exposed surface of the conductive feature, such that the recess is formed in the first layer in the region where the second layer is not covering the first layer, as required by claim 1 of the present invention.

Similalry, Ho fails to teach performing a preclean process on a surface of the first wiring level, wherein the preclean process forms a recess within the first layer in a region of the first wiring level where the second layer does not cover the first layer, and forming a second wiring level on a surface of the first wiring level comprising a third layer on the surface of the first wiring level and a plurality of conductive features within the third layer, wherein the recess within the first layer of the first wiring level is replicated producing an electrical short between at least two of the plurality of conductive features within the second wiring level, as required by claim 17 of the present invention.

Again, there is no mention in Ho of a preclean process forming a recess within the first layer. In addition, Ho does not teach forming a third layer on the surface of layer 12 having a plurality of conductive features, much less the replication of the recess formed in layer 14 that produces an electrical short between at least two conductive features within the third layer.

Therefore, Applicants respectfully maintain that Ho does not anticipate claims 1 and 17, and that claims 1 and 17 are in condition for allowance. Furthermore, since claims 2-12 depend from claim 1 and claims 19-21 depend from claim 17, Applicants contend that claims 2-12 and 19-21 are likewise in condition for allowance.

35 U.S.C. § 103

The Examiner rejected claim 3 under 35 U.S.C. §103(a) as allegedly being unpatentable over Ho in view of Demmin. Since claim 3 depends from claim 1, which Applicants have argued *supra* to be patentable under 35 U.S.C. §102, Applicants maintain that claim 3 is not unpatentable under 35 U.S.C. §103(a).

The Examiner rejected claims 7-12 under 35 U.S.C. §103(a) as allegedly being unpatentable over Ho in view of Hsieh. Since claims 7-12 depend from claim 1, which Applicants have argued *supra* to be patentable under 35 U.S.C. §102, Applicants maintain that claims 7-12 are not unpatentable under 35 U.S.C. §103(a).

Conclusion

Based on the preceding arguments, Applicants respectfully believe that claims 1-12, 17 and 19-21 and the entire application meet the acceptance criteria for allowance and therefore request favorable action. However, should the Examiner believe anything further is necessary in order to place the application in better condition for allowance, or if the Examiner believes that a telephone interview would be advantageous to resolve the issues presented, the Examiner is invited to contact the Applicants' undersigned representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,

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